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A Novel Asymmetrical Multilevel Inverter for Higher Output Voltage Levels

Jay Kumar Rajak[1], Padmini Katare[2]
[1]Student, [2]Assistant Professor
[1, 2]Department of Electrical & Electronics Engineering, MITS, Bhopal, India

Abstract: In this Paper focus on design and achievement of the new topology in a multilevel inverter with a reduction harmonic, size, cost in higher efficiency the main objective of this work a novel three-phase inverter with applicable in induction motor drive in medium voltage application. The main advantage of the new topology is to reduce the THD (Total Harmonic Distortion) lower electromagnetic interference generation and higher output voltage for applicable induction motor drive. This work describes a reduce harmonic in a single phase seven level, Twenty level & Twenty seven level inverter circuit with new level shift pulse width modulation (LSPWM) scheme is purposed. This topology is a combination of a three single level full bridge inverter circuit. There are many topologies of multilevel inverters in literature, popular among them are cascaded H-bridge. In general the control methods of these cascaded inverters are designed an assumption of having all dc source voltages same for all H-bridges. The performance of the purposed a novel seven, twenty three, and twenty seven level multilevel inverter with same number of H-bridges is modified with theinherent benefits & isolated DC sources, The multilevel carrier based Level shifted pulse width modulation methods are used in this topology a seven, twenty three, and twenty seven level output voltage wave forms is shown in FFT window. MATLABE/SIMULINK is used to simulate the inverter circuit operation and control signals.
Keywords—Two Level Inverter, Reduced Switches and Sources, Pulse Width Modulation (PWM), Multi-Level Inverters
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I. INTRODUCTION

The voltage cause inverters make a voltage or a current with levels likewise 0 or ±V dc they are notable as two level inverters. They require high exchanging recurrence alongside different heartbeat width balance (PWM) systems to get a quality result voltage or an ongoing waveform with a base measure of wave content, Encompassed by high power and high voltage application, these two phase inverters, then again, have a few limitations in working at high recurrence fundamentally because of exchanging gadgets ought to be utilized so as to avoid issues associated with their series-equal blends that are important to get capacity of taking care of high voltages and flows.

The staggered inverter [MLI] is a shows potential inverter geography for high voltage and high power applications. This inverter combines various degrees of DC voltages to deliver a flight of stairs with the reason for approaches the purifying waveform. It has high power predominance waveforms, lower voltage appraisals of gadgets, lower consonant twisting, lower exchanging recurrence and exchanging misfortunes, higher proficiency, and decrease of dt/dv stresses. It gives the chance of working with low speed semiconductors however its examination with the two-level inverter. a few of MLI geographies and balance methods have been presented and concentrated exhaustively. Yet, most acknowledged MLI geographies are Flowed Staggered Inverter (CMLI), Diode Clasp and Flying Capacitor. In this proposition we utilize a CMLI that comprise of some with not a similar DC named as Deviated Flowed Staggered Inverter (ACMLI) and H-Scaffold inverters. It is carried out in light of the fact that these inverters are more particular and straightforward in creation and have other prize than flying capacitor and Diode clasp. [2] [3]

II. LITERATUERE SURVEY

Staggered inverter is exceptionally adaptable and is utilizes for power gadgets geography for high power application. The staggered inverter has an exceptionally low electromagnetic obstruction (EMI), The voltage across the switches is just a single portion of the DC source voltage, The exchanging recurrence can be diminished for similar exchanging misfortunes, The higher result current sounds are decreased by a similar exchanging recurrence. It proficiency is high contrast with regular inverter. Staggered inverter is a latest choice to execute low recurrence based inverters with low result voltage bend. Essential staggered geographies are of three sorts.

1. Diode-Clasped Staggered Inverter
2. Capacitor Clipped/Flying Capacitor Inverter
3. Overflow H-span (CHB)

Each three geographies of a staggered inverter can be utilized in receptive power pay excluding having the voltage unbalance issue.

Diode clipping isn't ideal in quick capacitor and flowed inverter plan and adjusting capacitors are not needed in diode braced and flowed inverter design. In flowed inverter arrangement requires the littlest sum number of parts.

The diode braced geography is likewise called as an unbiased point converter. It was the main broadly well-known staggered inverter geography. It is extensively utilized in modern application this three levels unbiased point converter utilizes capacitor to produce middle voltage level and voltages across the switches are just half cycle in dc input. These inverters most normally utilized in medium power and high power voltages. In this inverter geography diode is utilized as the bracing gadget to clasp the dc transport voltage so equivalent to accomplish steps in the result voltage. Accordingly, the significant idea of this inverter is to utilize diodes to tie the power gadgets voltage stress. The voltage over every capacitor and each switch is V_{dc}.

A comparative geography to the Unbiased Point Clasped Staggered Inverter geography is the Capacitor Clipped (CC), or Flying Capacitor, staggered inverter geography, as a substitute of utilizing cinching diodes it utilizes capacitors to hold the voltages to the ideal qualities. With respect to the Impartial Point Clasped Staggered Inverter,(m-1) number of capacitors on a common DC-transport, where m is the level number of the inverter, and 2(m-1) switch-diode valve matches are utilized. Then again, for the CCMLI, rather than bracing diodes, at least one (contingent upon position and level of the inverter) capacitor are utilized to make the result voltages. They are associated with the midpoints of two valve matches on similar situation on each side of the midpoint between the valves [3].

Overflow H-bridge(CHB): Configuration has recently happen to extremely famous in movable speed drive and high-power AC supplies applications. In every one of its three stages, overflow staggered inverter contains of a progression of H-span (single-stage full scaffold) inverter units. Every one H-span unit has its own DC source, which for an enlistment engine would be a battery unit, sun based cell or energy component.

III. PROPOSED METHODOOGY

The graphic arrangement of the proposed block Diagram of Multi Level inverter is shown in figure - 1.

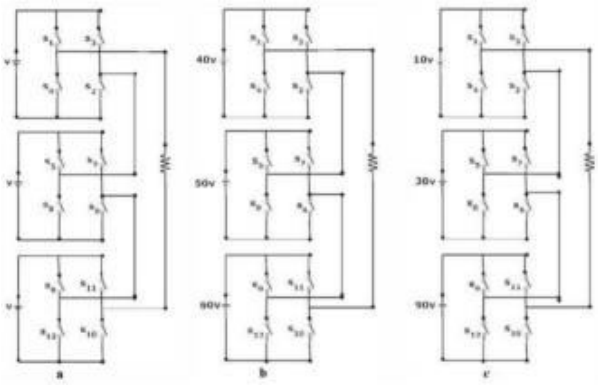

Figure-1 Proposed block diagram The DC-link is universal for all the phases.

Each phase consists of a three-level arrangement connected to common DC-link and a full-bridge with FC coupled at the output of three-level arrangement. Each D.C. source is connected with a singlephase full bridge inverter. The AC terminal voltages of different level inverters are linked in series. Each one converter level can generate three dissimilar voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero because of dissimilar combinations of the four switches, S1, S2, S3 and S4. The AC outputs of dissimilar full-bridge converters in the identical phase are attached in series such that the synthesized voltage waveform is the addition of the individual converter outputs. Note that the number of output-phase voltage levels is defined in a different way from those of the two earlier converters (i.e. diode clamped and flying capacitor). The number of output phase voltage levels is formulated by m= 2N+1, where N is the number of DC sources in this topology. A seven-level cascaded converter such that, contents of three full bridge converters and three DC sources. Minimum harmonic deformation can be obtained by controlling the conducting angles on different converter levels. Each H-bridge part generates a quasi-square waveform by phase changing its negative and positive phase legs switching timings. Each switching device for all time conducts 180° (or half cycle) apart from the pulse width of the quasi-square wave. All of the switching devices current stress equal because of this switching method. In the motoring manner, power flows from the batteries from side to side the cascade inverters to the motor.

The single phase seven level hybrids cascaded multilevel inverter diagram is given Figure 2 .this type of the inverter has two types: first one is H-bridge inverter and other is conventional inverter. The conventional inverter is acting the main inverter and H-bridge inverter is acting the auxiliary inverter. The Main inverter output voltage is either +Vdc/2 (S1isON) or -Vdc/2 (S2 is ON).its connected in series with a full H-bridge that in turn is supplied by a capacitor voltage. If the capacitor is kept charged to Vdc/2, then the output voltage of the H-bridge can take on the values +Vdc/2 (Sa3 &Sa6 ON), 0 (Sa3, Sa4, Sa5, Sa6 are ON) or -Vdc/2 (Sa4 & Sa5 ON)

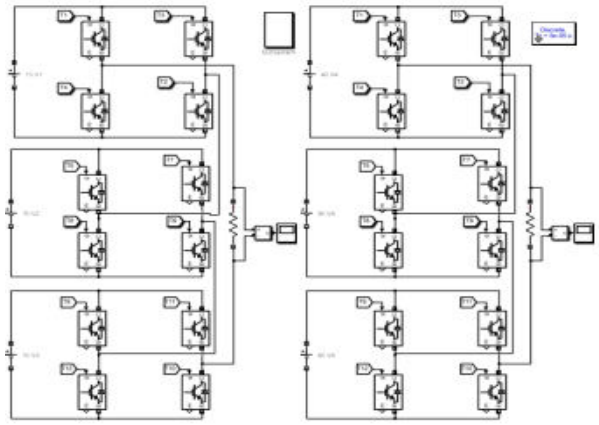

Figure 2: Single Phase Seven-level & Twenty three level H-bridge MLI simulation diagram

Table 1: Switching States of Seven-Level Inverter

Switches / Voltage Levels	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
V_{dc}	1	0	1	0	0	0	1	1	1	1	0	0
$2V_{dc}$	0	0	1	1	1	0	1	0	1	1	0	0
$3V_{dc}$	1	1	0	0	1	1	0	0	0	0	1	1
$4V_{dc}$	1	1	0	0	1	0	1	0	1	0	1	0
$5V_{dc}$	1	0	1	0	1	1	0	0	1	0	1	0
$6V_{dc}$	1	0	1	0	1	0	1	0	1	1	0	0
$7V_{dc}$	0	0	1	1	1	1	0	0	1	1	0	0
$9V_{dc}$	1	1	0	0	1	1	0	0	1	0	1	0
$10V_{dc}$	1	1	0	0	1	0	1	0	1	1	0	0
$11V_{dc}$	1	0	1	0	1	1	0	0	1	0	1	0
$15V_{dc}$	1	1	0	0	1	1	0	0	1	1	0	0
$0V_{dc}$	1	0	1	0	1	0	1	0	1	0	1	0
$-V_{dc}$	1	0	1	0	1	1	0	0	0	0	1	1
$-2V_{dc}$	1	1	0	0	1	0	1	0	0	0	1	1
$-3V_{dc}$	0	0	1	1	0	0	1	1	1	1	0	0
$-4V_{dc}$	0	0	1	1	1	0	1	0	1	0	1	0
$-5V_{dc}$	1	0	1	0	0	0	1	1	1	0	1	0
$-6V_{dc}$	1	0	1	0	1	0	1	0	0	0	1	1
$-7V_{dc}$	1	1	0	0	0	0	1	1	0	0	1	1
$-9V_{dc}$	0	0	1	1	0	0	1	1	1	0	1	0
$-10V_{dc}$	0	0	1	1	1	0	1	0	1	0	1	1
$-11V_{dc}$	1	0	1	0	0	0	1	1	0	0	1	1
$-13V_{dc}$	0	0	1	1	0	0	1	1	0	0	1	1

Table- 1 shows the current orders for different operating modes of seven-level & twenty three level inverter. Generation of pulse width modulation signal formula is shown in table 1. These pulses are given for 24 switches use. In this inverter has 12 switches “Sa1, Sa2, Sa3, Sa4, Sb1, Sb2, Sb3, Sb4Sc1, Sc2, Sc3, Sc4 “ for upper lag and 12 switches “ Sa11, Sa21, Sa31, Sa41 , Sb11, Sb21, Sb31, Sb41 ,Sc11, Sc21, Sc31, Sc41 for lower lag . The corresponding conducting switches and inverter output voltage levels are given in Table 2. It can be understand that the number of conducting switches for each level is very less. This ensures the higher efficiency of the proposed sevenlevel inverter.

Table 2: Conducting switches at different levels of output voltage

Switches / Voltage Levels	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
V_{dc}	1	1	0	0	0	1	0	1	0	1	0	1
$2V_{dc}$	0	0	1	1	1	1	0	0	0	1	0	1
$3V_{dc}$	0	1	0	1	1	1	0	0	0	1	0	1
$4V_{dc}$	1	1	0	0	1	1	0	0	0	1	0	1
$5V_{dc}$	0	0	1	1	0	0	1	1	1	1	0	0
$6V_{dc}$	0	1	0	1	0	0	1	1	1	1	0	0
$7V_{dc}$	1	1	0	0	0	0	1	1	1	1	0	0
$8V_{dc}$	0	0	1	1	0	1	0	1	1	1	0	0
$9V_{dc}$	0	1	0	1	0	1	0	1	1	1	0	0
$10V_{dc}$	1	1	0	0	0	1	0	1	1	1	0	0
$11V_{dc}$	0	0	1	1	1	1	0	0	1	1	0	0
$12V_{dc}$	0	1	0	1	1	1	0	0	1	1	0	0
$13V_{dc}$	1	1	0	0	1	1	0	0	1	1	0	0
$0V_{dc}$	0	1	0	1	0	1	0	1	0	1	0	1
$-V_{dc}$	0	0	1	1	0	1	0	1	0	1	0	1
$-2V_{dc}$	1	1	0	0	0	0	1	1	0	1	0	1
$-3V_{dc}$	0	1	0	1	0	0	1	1	0	1	0	1
$-4V_{dc}$	0	0	1	1	0	0	1	1	0	1	0	1
$-5V_{dc}$	1	1	0	0	1	1	0	0	0	0	1	1
$-6V_{dc}$	0	1	0	1	1	1	0	0	0	0	1	1
$-7V_{dc}$	0	0	1	1	1	1	0	0	0	0	1	1
$-8V_{dc}$	1	1	0	0	0	1	0	1	0	0	1	1
$-9V_{dc}$	0	1	0	1	0	1	0	1	0	0	1	1
$-10V_{dc}$	0	0	1	1	0	1	0	1	0	0	1	1
$-11V_{dc}$	1	1	0	0	0	0	1	1	0	0	1	1
$-12V_{dc}$	0	1	0	1	0	0	1	1	0	0	1	1
$-13V_{dc}$	0	0	1	1	0	0	1	1	0	0	1	1

IV. SIMULATION RESULTS

The below figure shows the output wave forms the proposed asymmetrical converter. It is clearly seen that the level of inverter varies with the change in the ratios of input voltage.

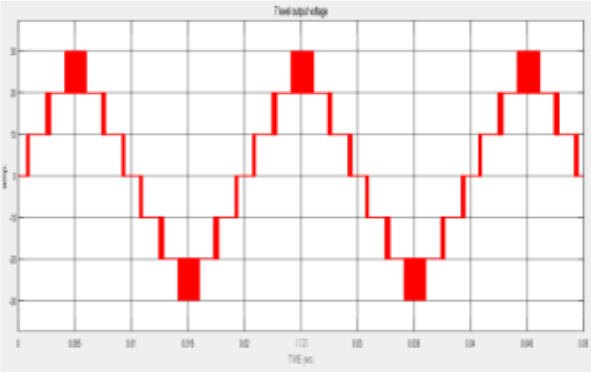

Figure 3: output voltage waveform of seven levels

Switching of the converter is done by following the staircase control technique. Pulse width ML Modulation technique can also be applied by appropriate calculation of the switching time period.

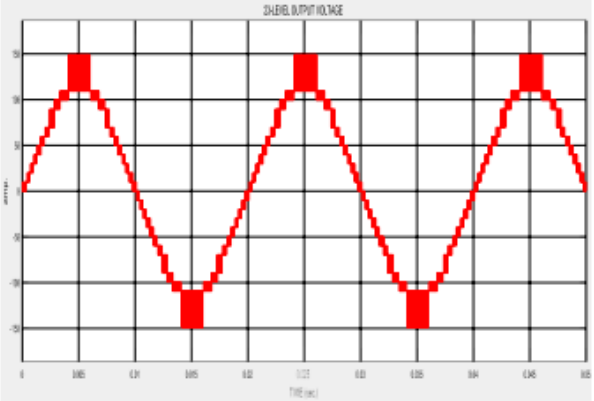

Figure 4: output voltage waveform of twenty three levels MLI

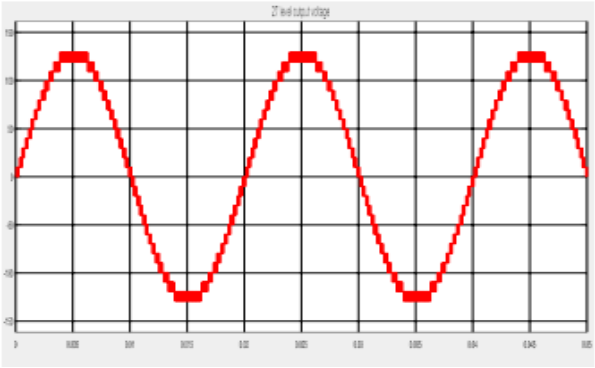

Figure 5: output voltage waveform of twenty seven levels MLI

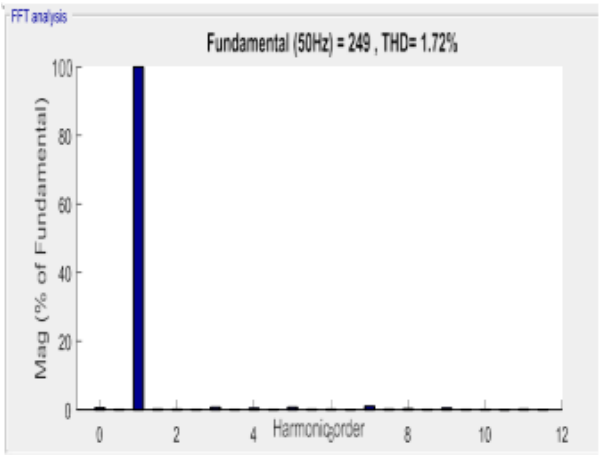

Figure 6: FFT analysis of new seven levels MLI output voltage waveform

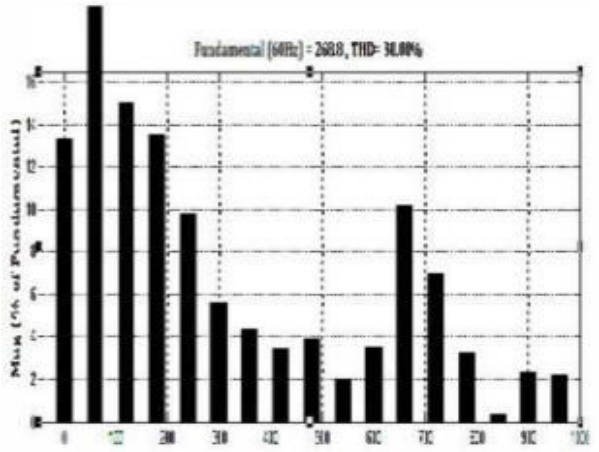

Figure 7: FFT analysis of Old seven levels MLI output voltage waveform.

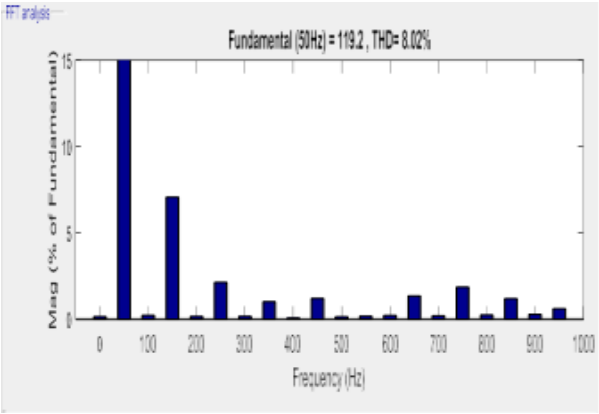

Figure 8: FFT analysis of New Twenty three levels MLI output voltage waveform

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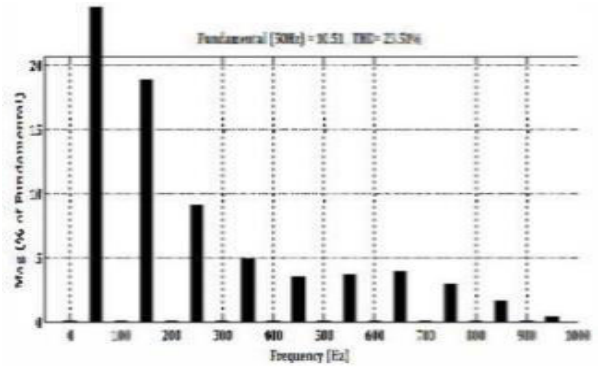

Figure 9: FFT analysis of Old Twenty three levels MLI output voltage waveform

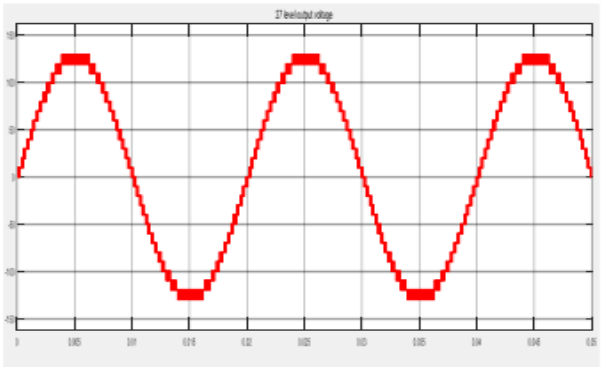

Figure 12: output voltage waveform of twenty seven levels MLI with Induction Motor

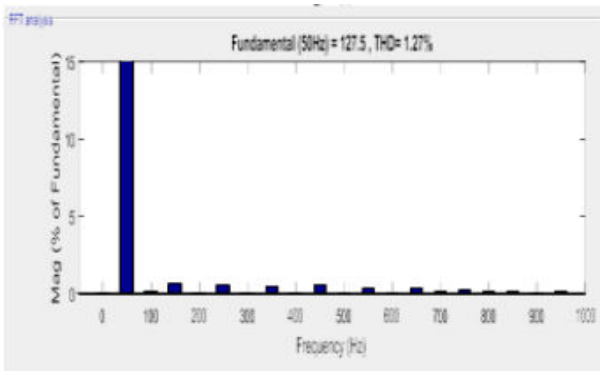

Figure 10: FFT Analysis of New Twenty Seven leves MLI output voltage waveform

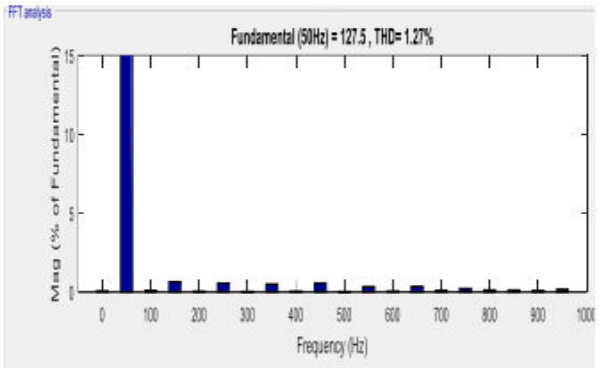

Figure 13: FFT analysis for Old twenty seven levels MLI with Induction Motor Load fed.

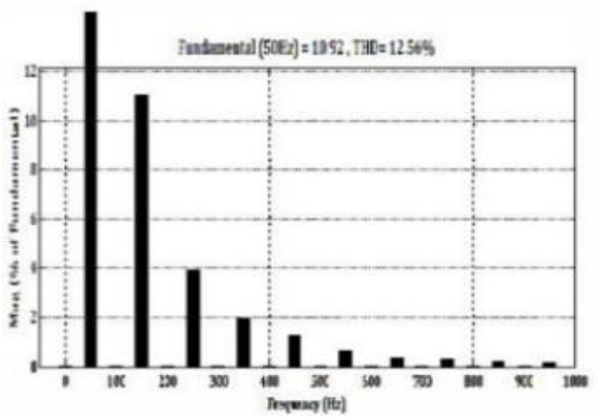

Figure 11: FFT analysis of OD Twenty Seven leves MLI output voltage waveform

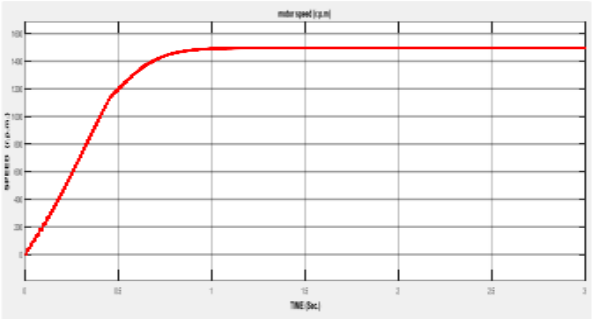

Figure 14: Speed characteristics of new MLI fed induction motor load

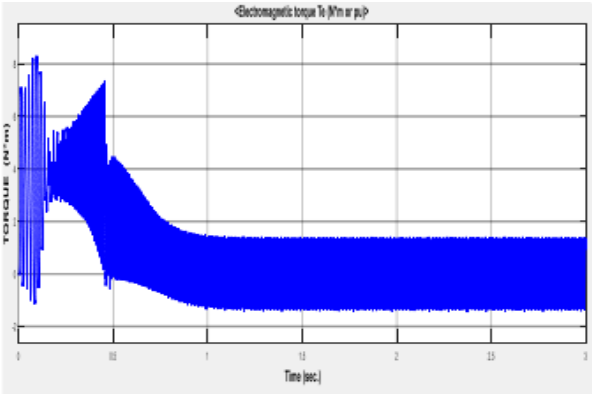

Figure 15: Torque characteristics of new MLI fed induction motor load.

Proposed H-bridge cascaded multilevel inverter circuit. The topology of an inverter circuit is based on the requirement and range. All topologies have both advantages and disadvantages. The two level inverters cost is very low as compared to other conventional inverter topologies. But very high value of THD. Then to reduce THD levels of a inverter voltage waveforms should be increased. And the number of level increases in a inverter then switching losses increased. Theses all above problems can be avoided by hybrid multilevel inverter. Figure 12 & Fig.-13 Shows in New & Old (Base paper) THD (total harmonics distortion) value for a proposed 3- Phase H-bridge cascaded multilevel inverter circuit with induction motor load in a seven level. This proposed circuit has THD-11.67% for a seven level output voltage waveform. The topology of an inverter circuit is based on the requirement and range. Figure 15 Speed Torque Characteristics of 3-phase IM for a proposed H-bridge cascaded multilevel inverter circuit in a seven level. Fig,-10 shows proposed circuit THD-11.67% & fig-11 shows old (base paper) circuits THD-24.57% for a seven level output voltage waveform.

V. CONCLUSIONS

This Paper work has provided a brief summary of implementation 7, 23 & 27- level multilevel inverter circuit is proposed for more improved output as per the requirement. In this proposed circuit output value of the voltage & THD is minor difference with motor load or without motor load shown result. Then also the power quality is improved & converter is large stable. Comparison a (Base paper) Old & New MLI without motor load results in 7, 23, & 27 levels HMLI shown in Table-3.

H-Bridge Inverters	Base paper THD	New THD	Base paper Fundamental Vol, (50 Hz)	New Fundamental Vol, (50 Hz)
7-level	30.07%	12.39 %	20.88 V.	22.94 V.
23-level	23.5 %	8.02 %	90.51 V.	119.2 V.
27-level	12.56 %	1.72 %	109.2 V.	127.5 V

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